Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the above-identified application:

- Please cancel claims 1-41 without prejudice.

Listing of Claims

1-41. **(Canceled)**

42. **(Original)** A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly comprising one or more regions, wherein at least one of the regions is an oxide region;

forming a passivation layer on a surface of the oxide region;

depositing a layer of metal material over the passivation layer; and

thermally treating the substrate assembly, wherein the passivation layer substantially prevents formation of a metal oxide at the oxide region during thermal treatment.

43. **(Original)** The method according to claim 42, wherein forming the passivation layer comprises exposing the surface of the oxide region to a nitrogen containing plasma.

44. **(Original)** The method according to claim 43, wherein the nitrogen containing plasma comprises one or more compounds selected from the group consisting of N_2, NH_3, NH=NH, and NH_2-NH_2.

45. **(Original)** The method according to claim 42, wherein the passivation layer comprises $Si_xO_yN_z$.

46. **(Original)** The method according to claim 42, wherein thermally treating the substrate assembly comprises performing a rapid thermal process on the substrate assembly at a temperature ranging between approximately 400 °C and 1,000 °C for a duration of time ranging between approximately 20 seconds and 2 minutes.

47. **(Original)** The method according to claim 42, wherein depositing the layer of metal material comprises depositing a titanium layer.

48. **(Original)** The method according to claim 47, wherein depositing the titanium layer comprises depositing the titanium layer to a thickness ranging from about 100 Å to about 500 Å.

49. **(Original)** The method according to claim 42, wherein the layer of metal material is deposited by a process selected from the group consisting of sputter deposition, chemical vapor deposition, physical vapor deposition, thermal evaporation, electron evaporation, and combinations thereof.

50. **(Original)** The method according to claim 42, wherein the passivation layer has a thickness ranging between about 10 Å and about 100 Å.

51. **(Original)** A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly comprising an oxide region and a non-oxide region;

forming a passivation layer on a surface of the oxide region;

depositing a layer of metal material over the passivation layer and the non-oxide region; and

thermally treating the substrate assembly, wherein the passivation layer substantially prevents formation of a metal oxide between the layer of metal material and the oxide region during thermal treatment.

52. **(Original)** The method according to claim 51, wherein forming the passivation layer comprises exposing the surface of the oxide region to a nitrogen containing plasma.

53. **(Original)** The method according to claim 52, wherein the nitrogen containing plasma comprises nitrogen in a range of about 10 sccm to about 5,000 sccm.

54. **(Original)** The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises exposing the surface to a pressure ranging between about 0.1 Torr and about 10 Torr.

55. **(Original)** The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises exposing the surface to a temperature ranging between about 100 °C and about 500 °C.

56. **(Original)** The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises providing power associated with the plasma ranging between about 300 Watts and about 3000 Watts.

57. **(Original)** The method according to claim 52, wherein exposing the surface of the oxide region to the nitrogen containing plasma comprises exposing the surface for a period of time ranging between about 20 seconds and about 600 seconds.

58. **(Original)** The method according to claim 51, wherein depositing the layer of metal material comprises depositing a titanium layer.

59. **(Original)** A method for use in the fabrication of a semiconductor device, the method comprising:

providing a substrate assembly including an oxide region and a silicon region;

exposing a surface of the oxide region to a plasma comprising nitrogen so as to form a passivation layer over the surface;

depositing a layer of titanium over the passivation layer and the silicon region; and

performing a thermal treatment on the substrate assembly, wherein the passivation layer substantially prevents formation of titanium oxide between the layer of titanium and the oxide region during thermal treatment.

60. **(Original)** The method according to claim 59, wherein the plasma comprises N_2 or NH_3.

61. **(Original)** The method according to claim 59, wherein the plasma comprises nitrogen in a range of about 10 sccm to about 5,000 sccm.

62. **(Original)** The method according to claim 59, wherein performing the thermal treatment comprises performing a rapid thermal process.

63. **(Original)** The method according to claim 62, wherein the rapid thermal process is performed at a temperature ranging between approximately 400 °C and approximately 1,000 °C.

64. **(Original)** The method according to claim 59, wherein performing the thermal treatment comprises annealing the substrate assembly at a temperature ranging between approximately 500 °C and approximately 1,000 °C.

65. **(Original)** The method according to claim 59, wherein the passivation layer comprises $Si_xO_yN_z$.

66. **(Original)** The method according to claim 59, wherein the passivation layer has a thickness ranging between about 10 Å and about 100 Å.

67. **(Original)** The method according to claim 59, wherein performing the thermal treatment comprises performing a rapid thermal nitridation process resulting in formation of a titanium silicide layer on the silicon region.